ABSTRACT OF THE DISCLOSURE

Embodiments of the present invention are broadly directed to a memory system. In one embodiment, a first data memory is coupled to a first memory controller and a second data memory is coupled to a second memory controller. A parity memory is coupled to a parity controller, the parity controller being directly coupled to both the first memory controller and the second memory controller. Parity data control logic is configured to store and retrieve parity information associated with data stored in both the first data memory and the second data memory, the parity data control logic configured to interleave within the parity memory parity data associated with data stored in the first data memory with parity data associated with data stored in the second data memory.